Listing of Claims

The following listing of claims will replace all prior versions, and listings, of claims in the subject application:

Claims 1-2 (canceled).

3. (previously presented) A subcode-data generating circuit, which generates subcode data including subcode component data which indicates time information and additional subcode component data which indicates information other than the time information, said circuit comprising:

a first generating portion for automatically generating the subcode component data which indicates the time information;

a second generating portion for automatically generating the additional subcode component data which indicates the information other than the time information;

a selecting portion which selects an output of at least one of said first and second generating portions; and

a memory,

wherein said first generating portion operates according to a first command for automatic generation of a plurality of time information subcode component data,

wherein said second generating portion operates according to a second command for automatic generation of a plurality of additional subcode component data, and

wherein the first commands are written collectively in a first area of said memory, and the second commands are written collectively in a second area of said memory, and

wherein each of said first commands written in said memory includes specification of a corresponding number of generation cycles.

4. (previously presented) The subcode-data generating circuit, as claimed in claim 3, wherein:

said second generating portion comprises a plurality of generating portions provided separately;

said second area of said memory comprises a plurality of areas corresponding to said plurality of generating portions; and

commands of the second commands are written collectively in each area of said plurality of areas, which commands correspond to a respective one of said plurality of generating portions.

Claim 5-7 (canceled).

8. (previously presented) The subcode-data generating circuit of claim 3, wherein each first command triggers automatic generation of two or more subcode component data.

9. (previously presented) The subcode-data generating circuit of claim 3, wherein said first and second generating portions operate independently, and the first generating portion continues to generate automatically the subcode component data which indicates the time information even when the second generating portion is not automatically generating the additional subcode component data which indicates the information other than the time information.

10. (previously presented) The subcode-data generating circuit of claim 3, wherein said each of said first commands written in memory further includes specification of a generation commencement sector.

11. (previously presented) The subcode-data generating circuit of claim 3, wherein said each of said second commands written in memory includes specification of a corresponding number of generation cycles

12. (previously presented) The subcode-data generating circuit of claim 11, wherein said each of said second commands written in memory includes specification of a generation commencement sector.

Claims 13-16 (canceled).